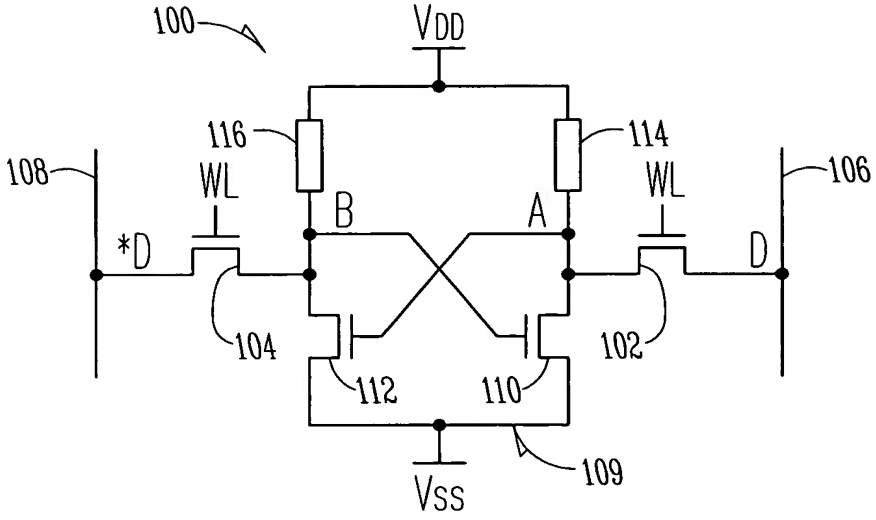

Fig. 1
(Prior Art)

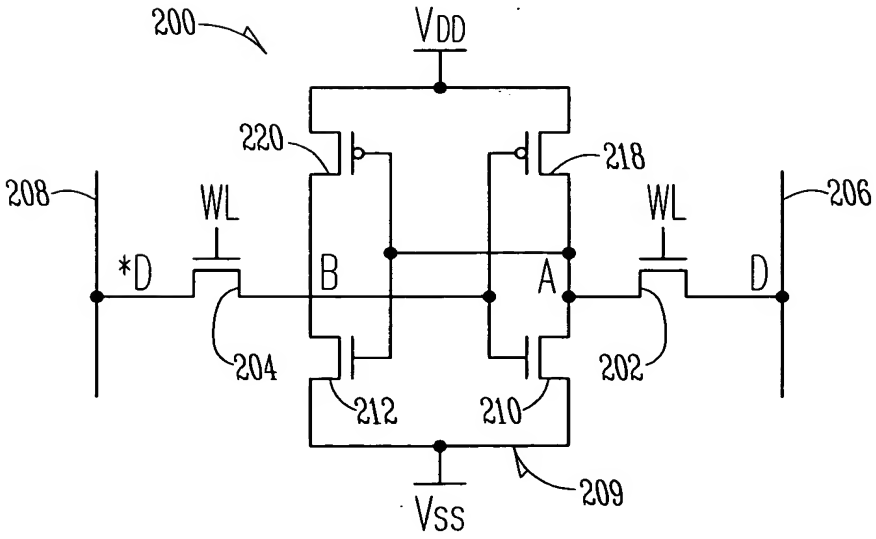

Fig. 2
(Prior Art)

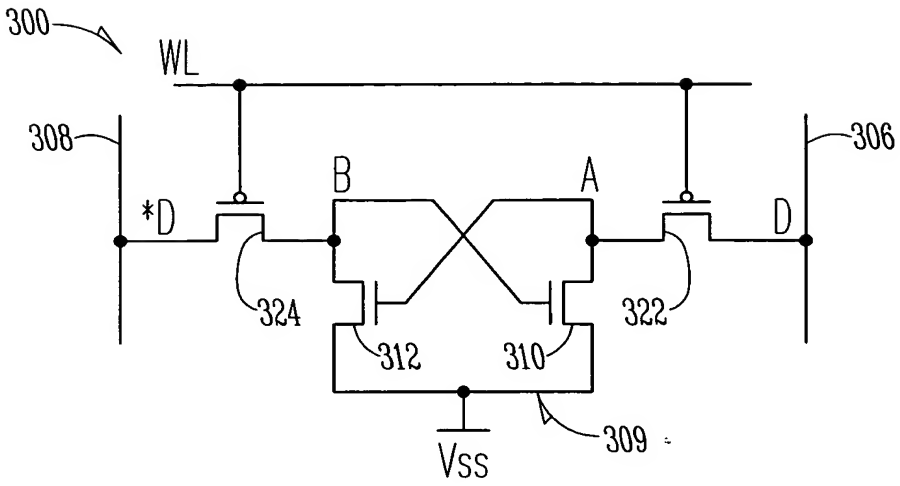

Fig. 3
(Prior Art)

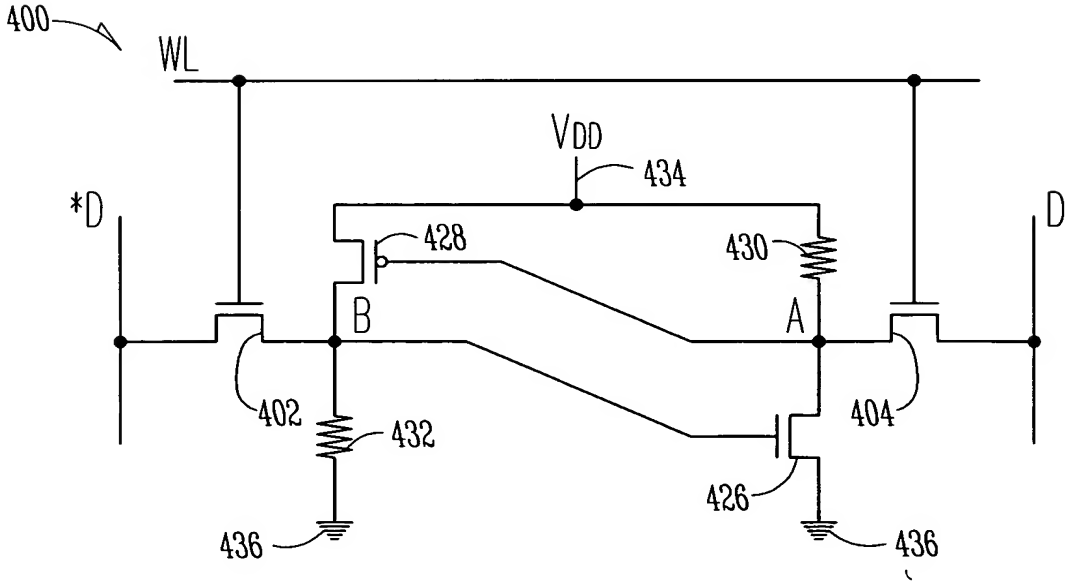

Fig. 4

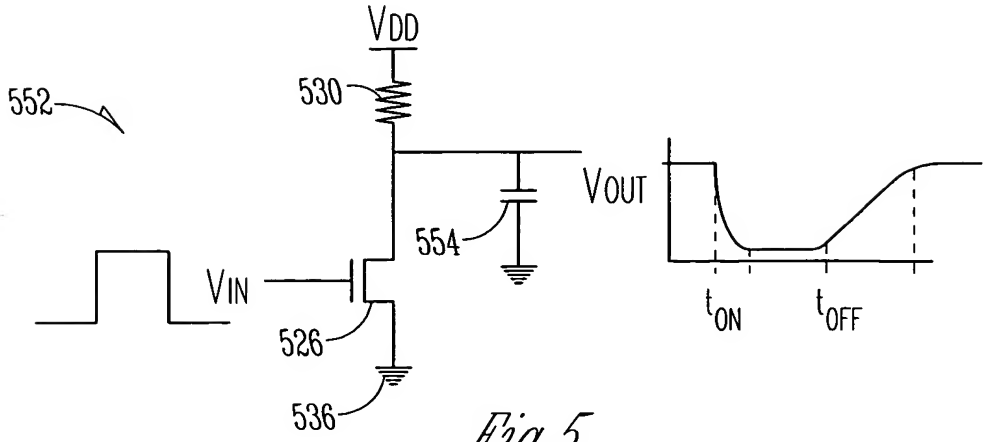

Fig. 5

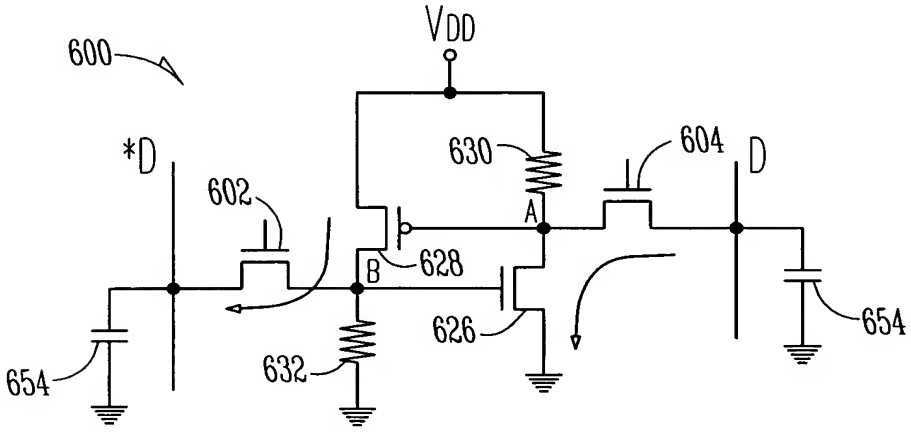

Fig. 6

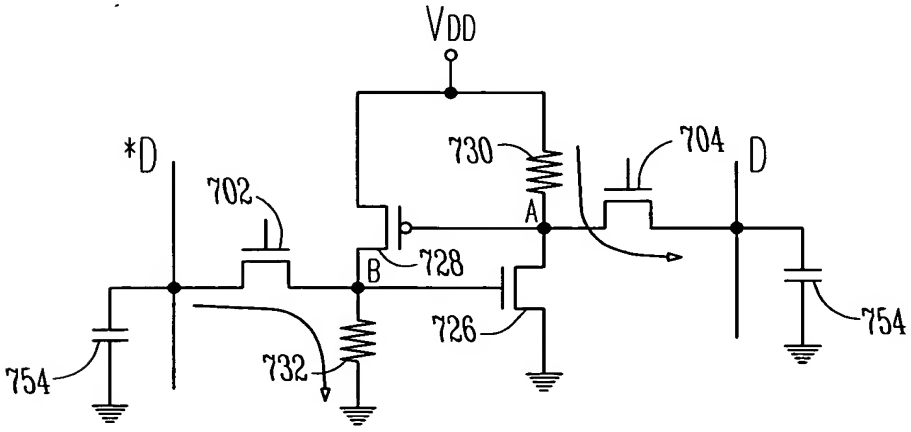

Fig. 7

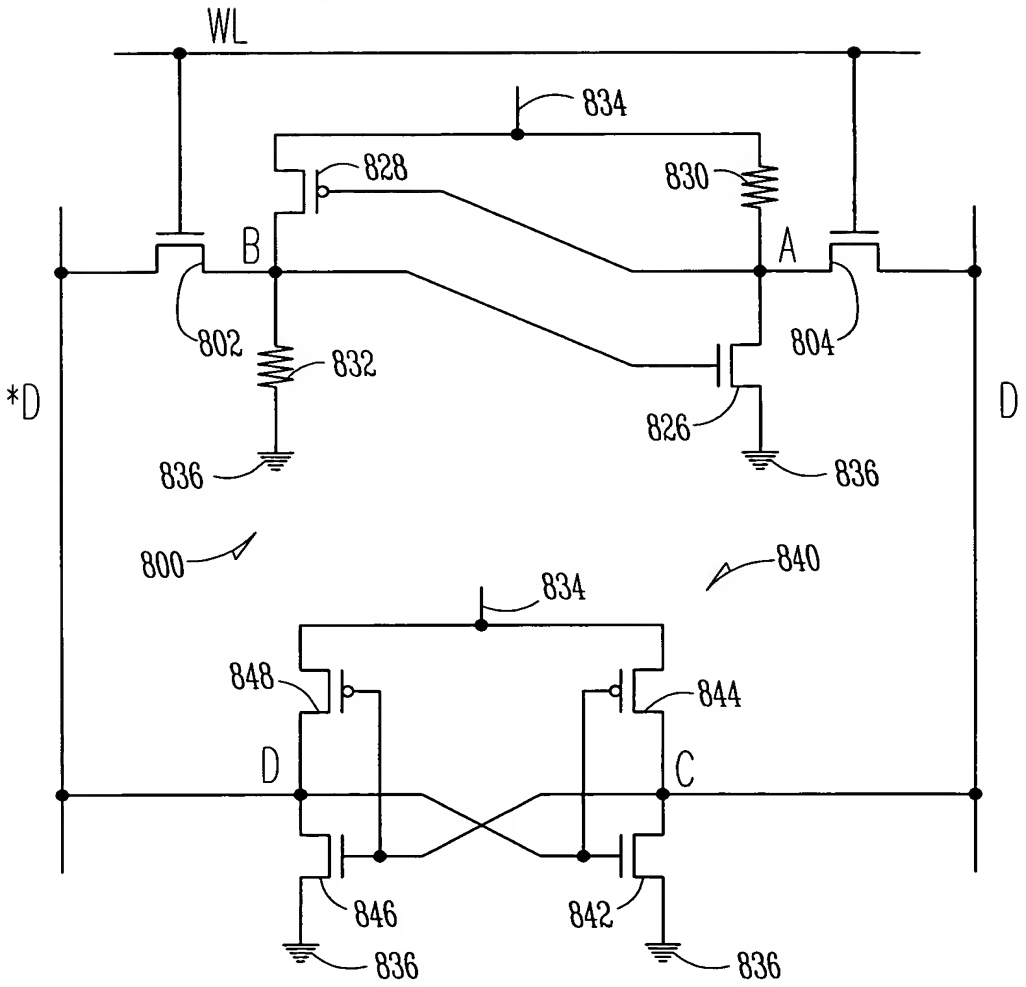
WL
834
828
830
B
A
802
804
832
*D
D
826
836
836
800
840
834
848
844
D
C
846
842
836
836

Fig. 8

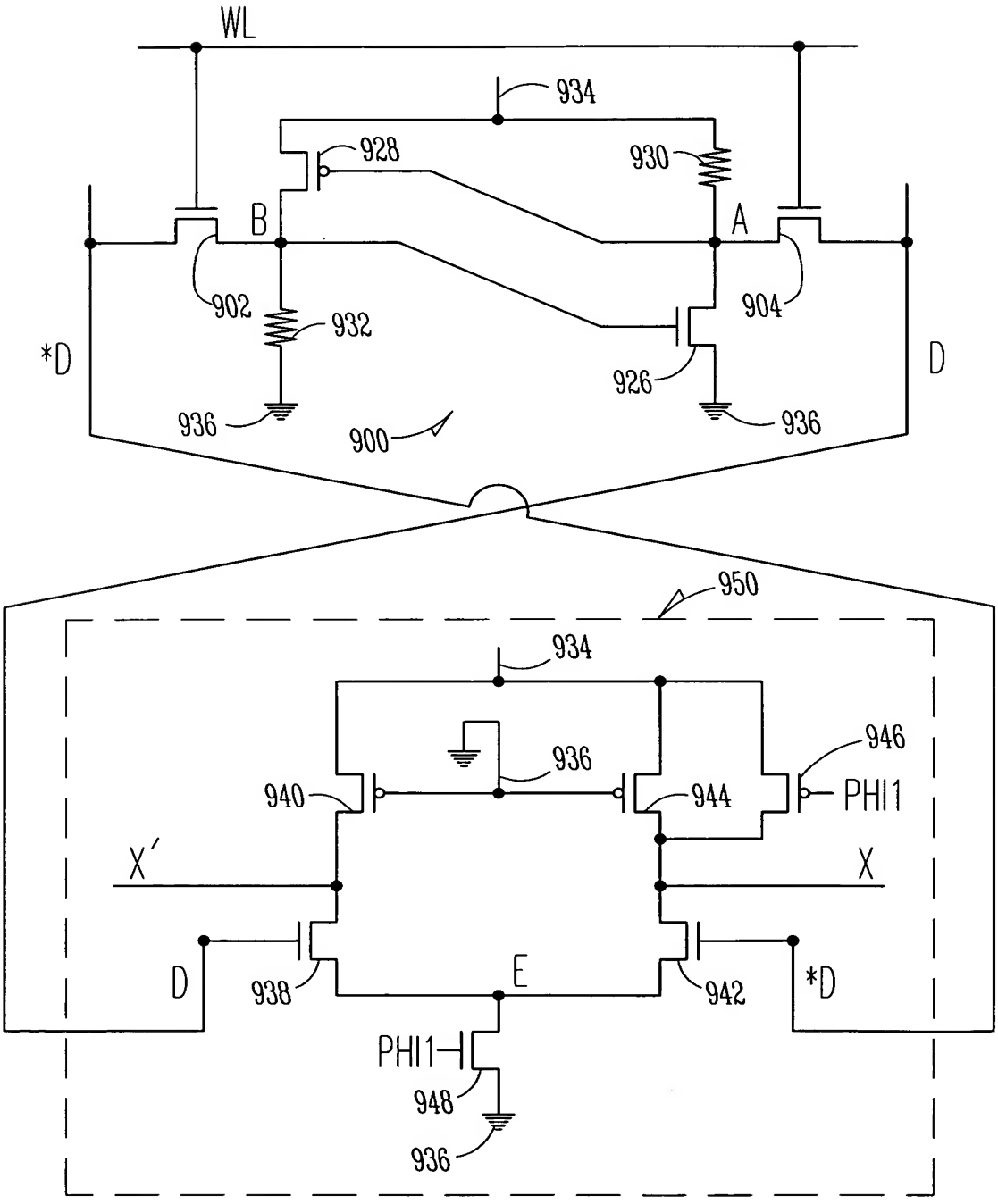
WL
934
928
930
B
A
902
932
904
*D
D
926
936
936
900
950
934
936
946
940
944
PHI1
X'
X
D
938
E
942
*D
PHI1
948
936

Fig. 9

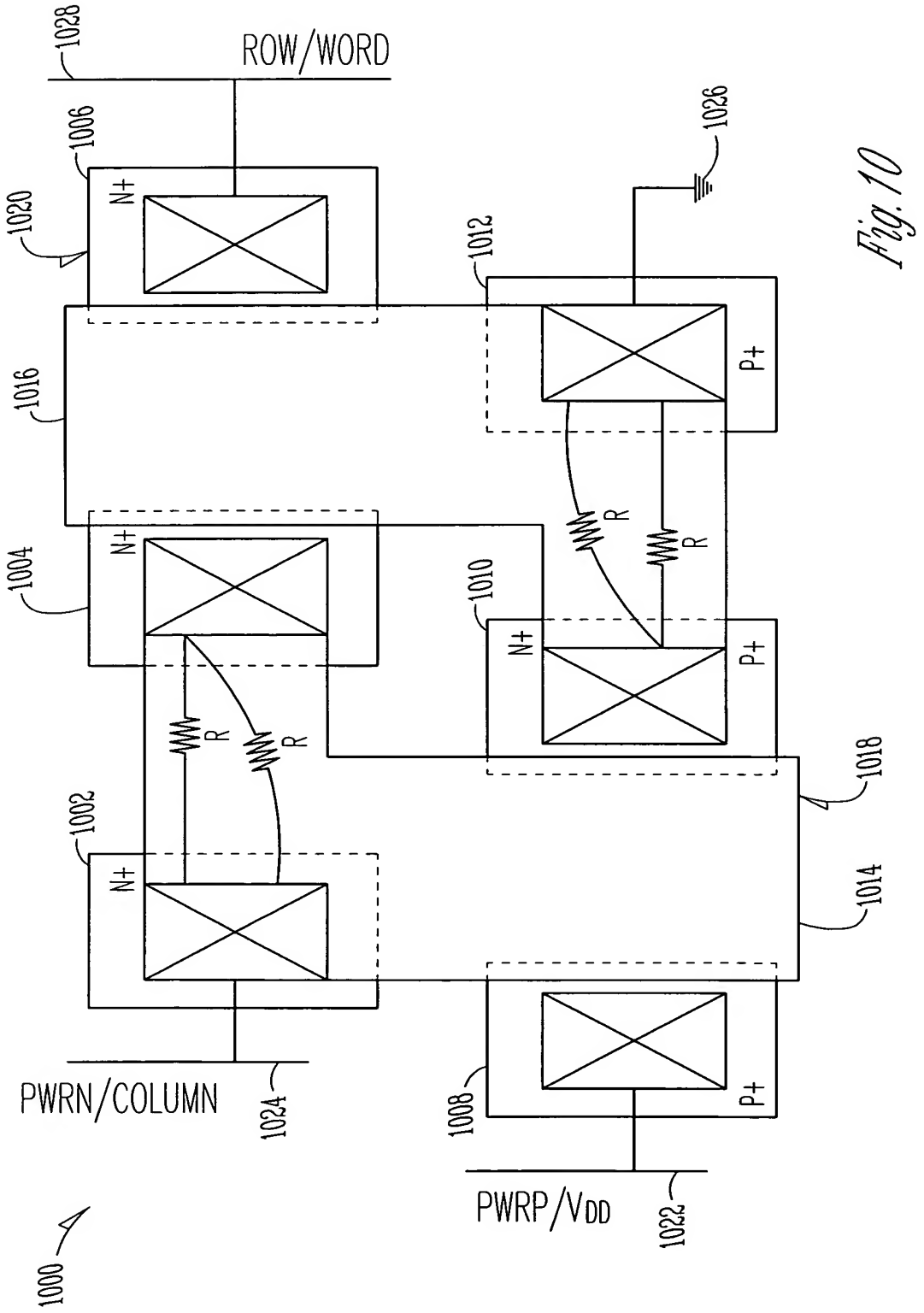
1028
ROW/WORD
1006
N+
1020
1026
1012
P+
1016
R
R
1004
N+
1010
N+
P+
R
R
1018
1002
N+
1014
PWRN/COLUMN
1024
1008
P+
PWRP/VDD
1022
1000

Fig. 10

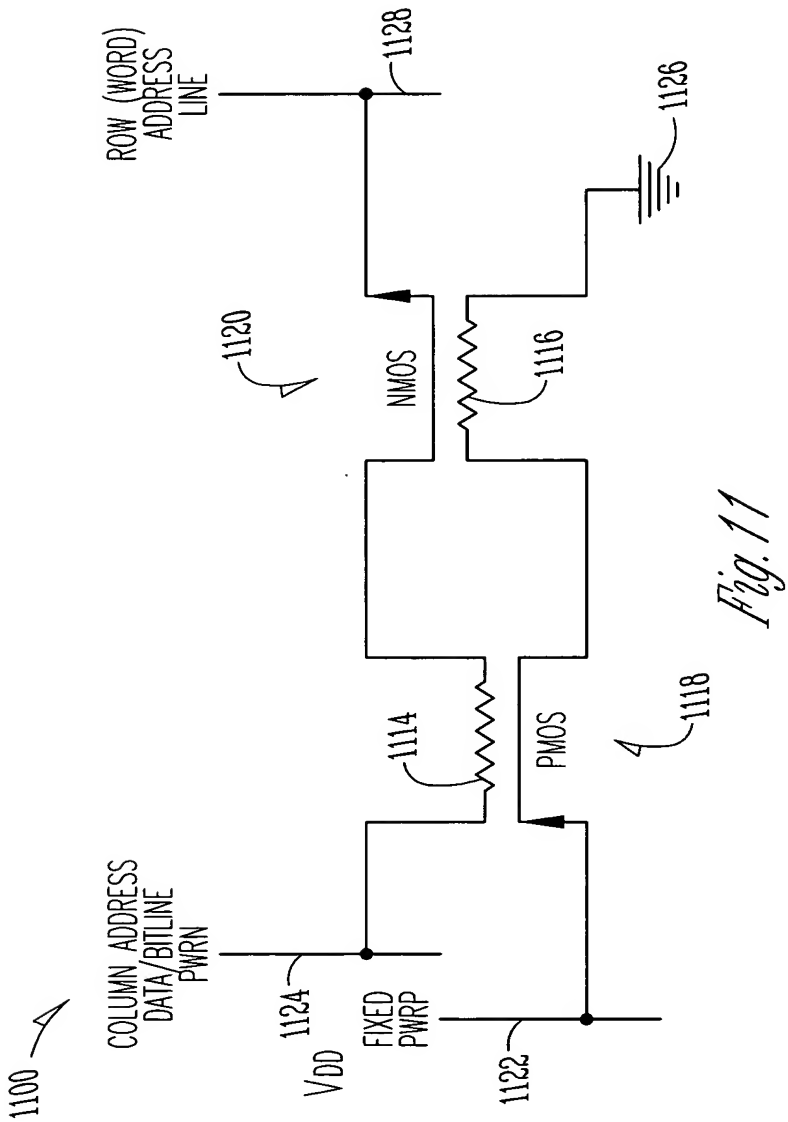
ROW (WORD) ADDRESS LINE
1128
1126
1120
NMOS
1116
1114
PMOS
1118
COLUMN ADDRESS DATA/BITLINE PWRN
1124
VDD
FIXED PWRP
1122
1100

Fig. 11

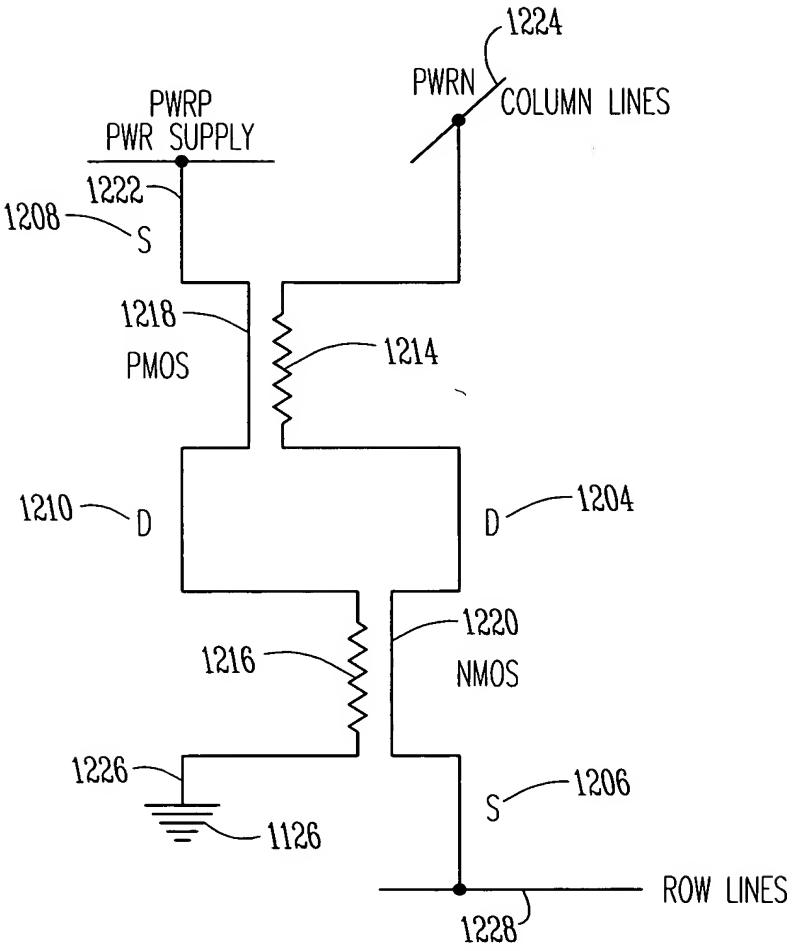
1224
PWRN
COLUMN LINES
PWRP
PWR SUPPLY
1222
1208
S
1218
PMOS
1214
1210
D
D
1204
1220
NMOS
1216
1226
1126
S
1206
ROW LINES
1228

Fig. 12

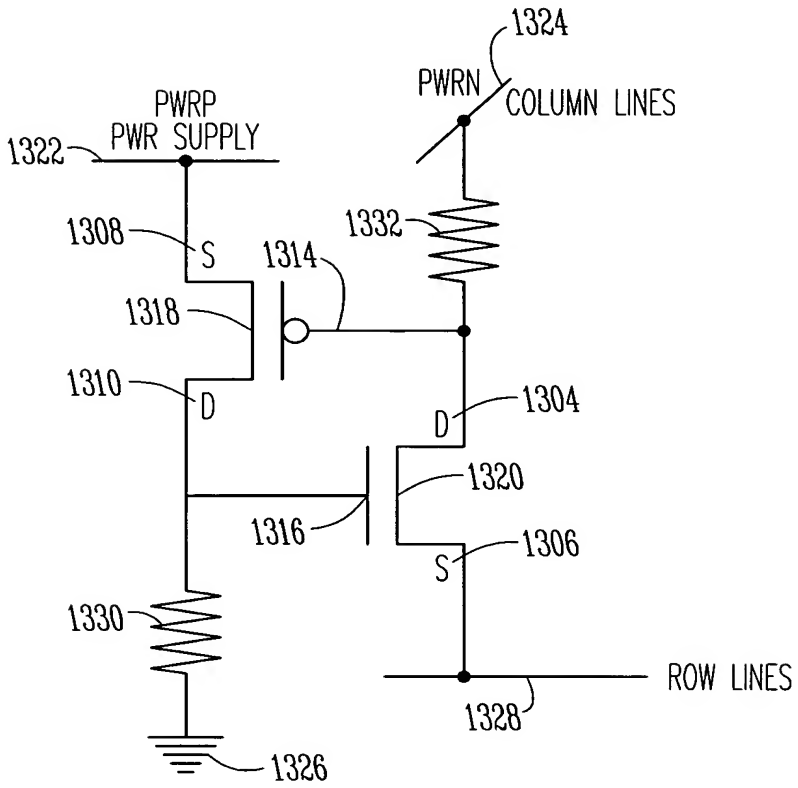
1324
PWRN
COLUMN LINES
PWRP
PWR SUPPLY
1322
1308
S
1314
1332
1318
1310
D
D
1304
1320
1316
1306
S
1330
ROW LINES
1328
1326

Fig. 13

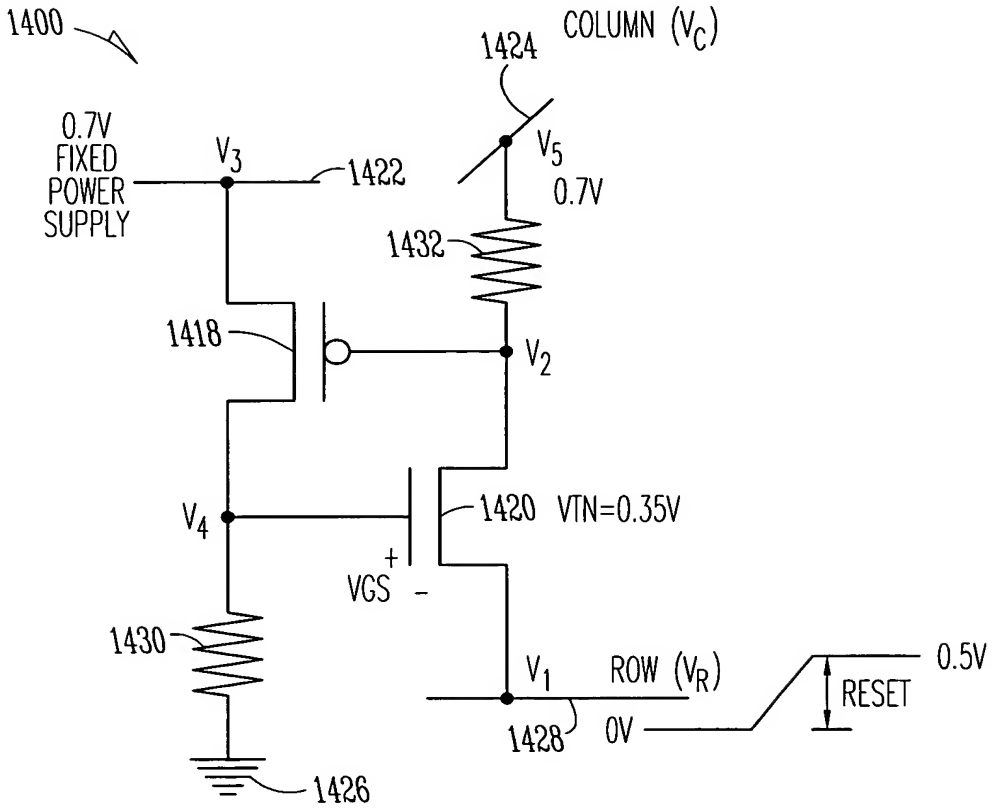
1400
COLUMN (V_C)
1424
0.7V
FIXED
POWER
SUPPLY
V_3
1422
V_5
0.7V
1432
1418
V_2
V_4
1420 VTN=0.35V
+
VGS
-
1430
V_1
ROW (V_R)
0.5V
RESET
1428
0V
1426

Fig. 14

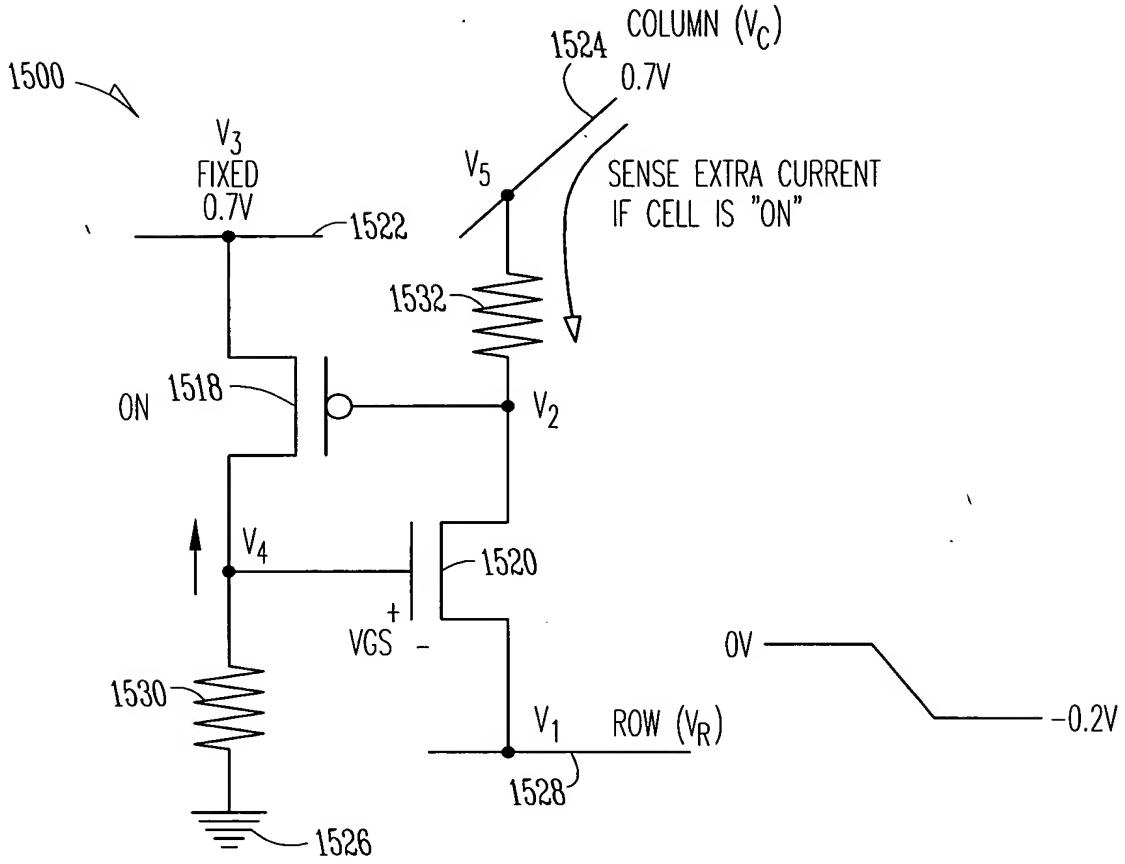
1500
V_3
FIXED
0.7V
1522
1524
COLUMN (V_C)
0.7V
V_5
SENSE EXTRA CURRENT
IF CELL IS "ON"
1532
ON
1518
V_2
V_4
1520
+
VGS
-
1530
0V
-0.2V
V_1
ROW (V_R)
1528
1526

Fig. 15

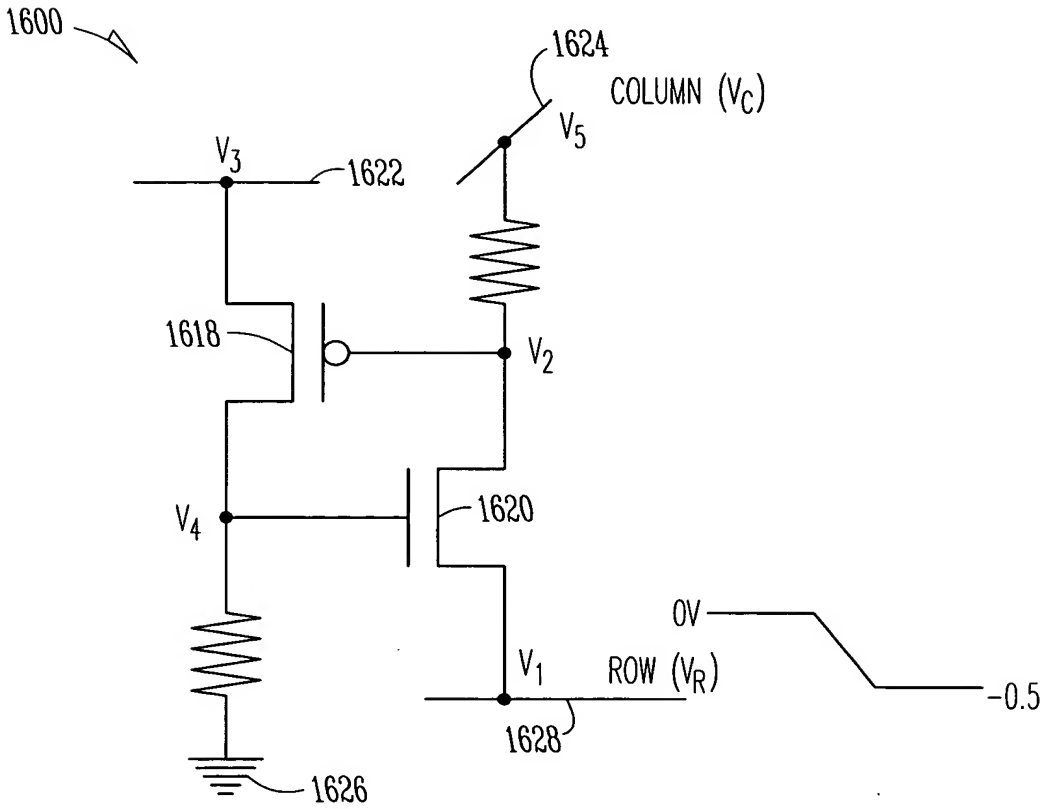
1600
1624
COLUMN (V_C)
V_5
V_3
1622
1618
V_2
V_4
1620
0V
V_1
ROW (V_R)
-0.5
1628
1626

Fig. 16a

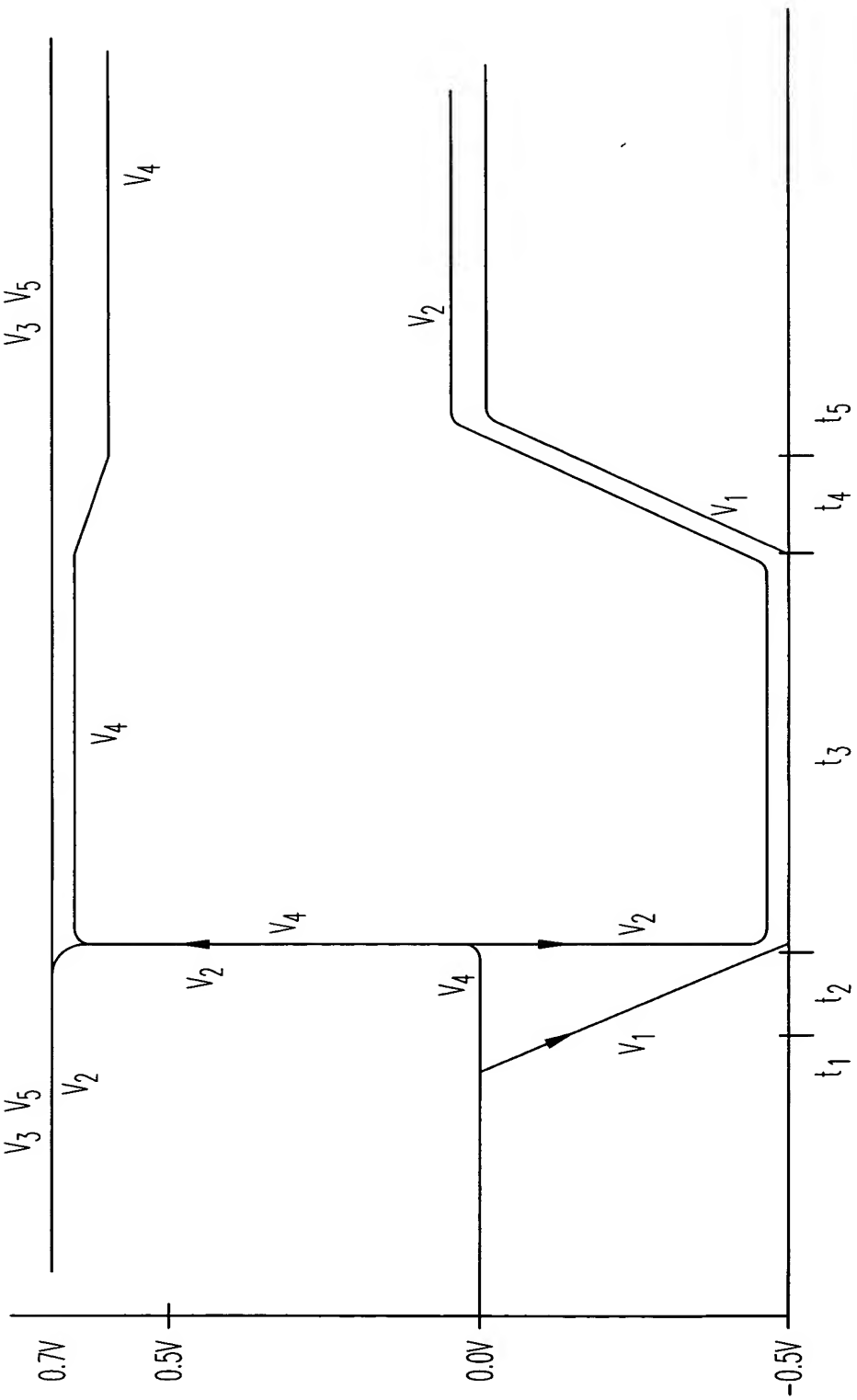

Fig. 16b

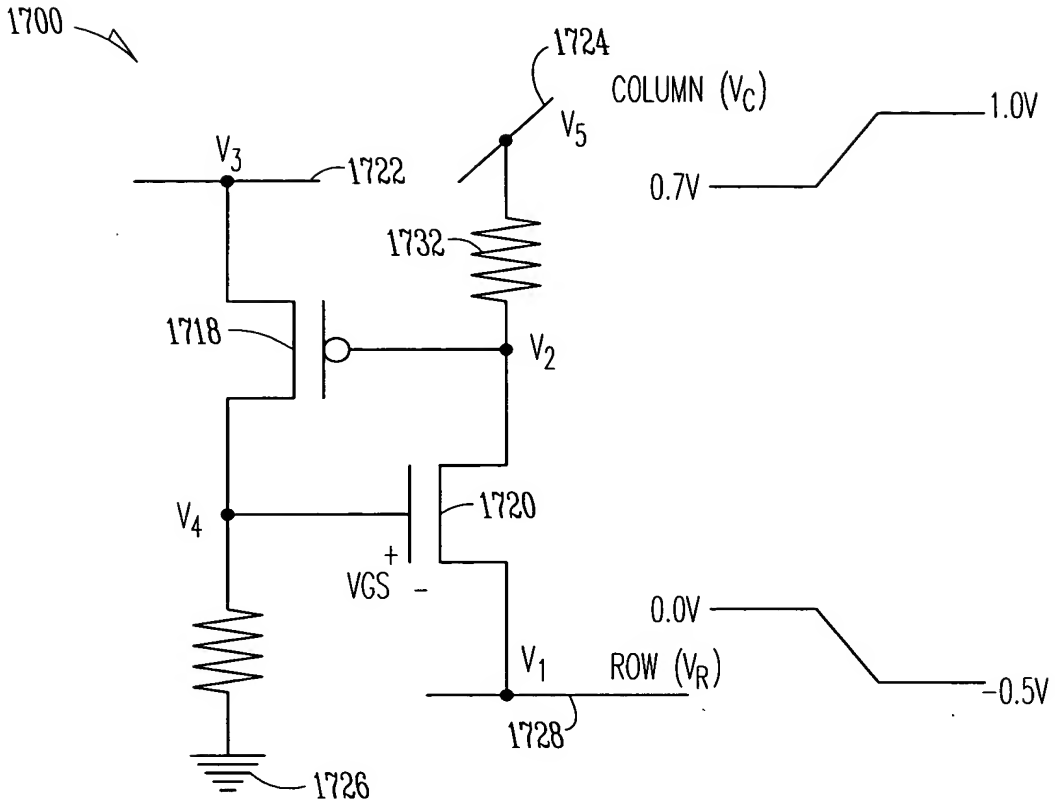
1700
1724
COLUMN (V_C)
1.0V
V_5
V_3
1722
0.7V
1732
1718
V_2
V_4
1720
+
VGS
-
0.0V
V_1
ROW (V_R)
-0.5V
1728
1726

Fig. 17a

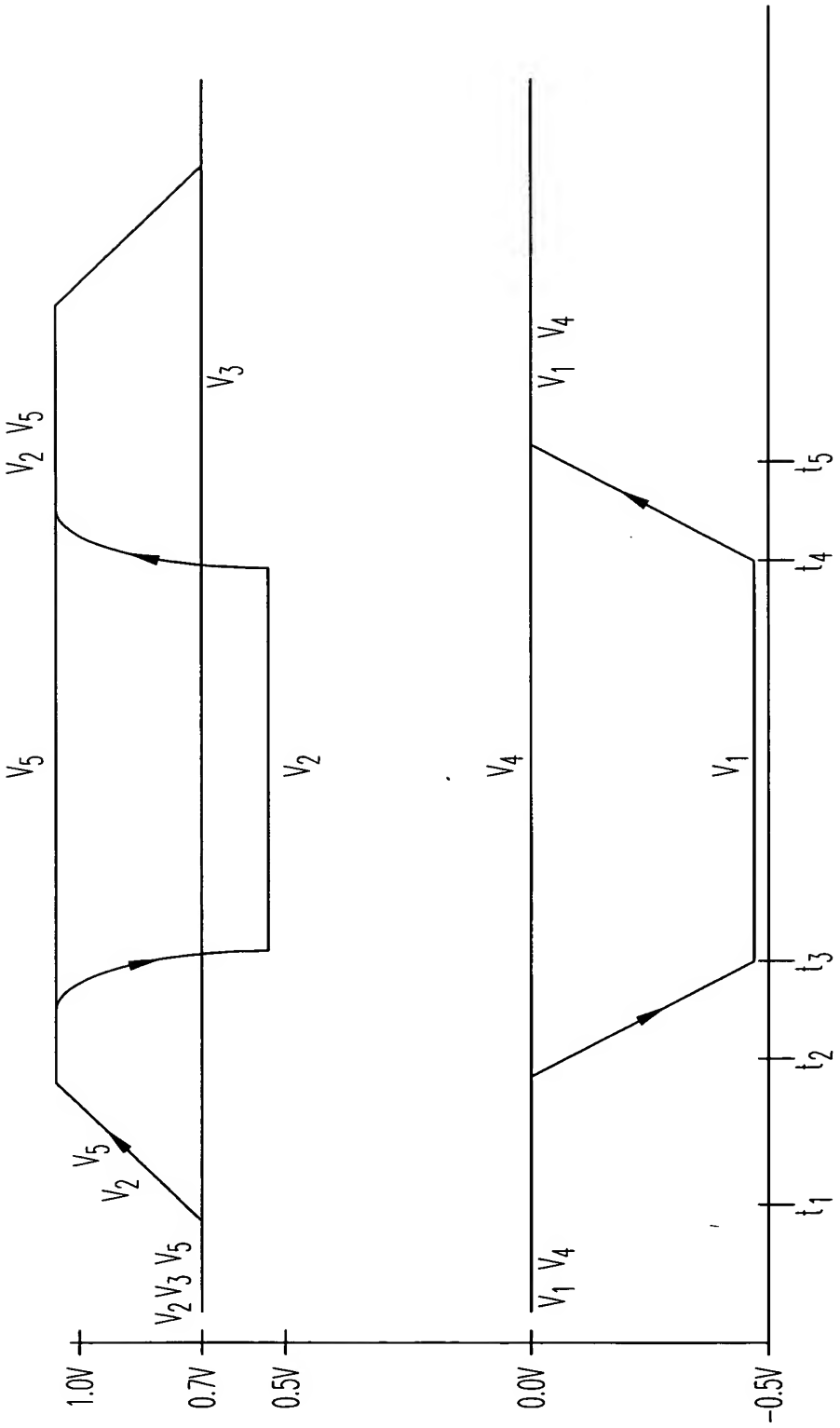
1.0V
0.7V
0.5V
0.0V
-0.5V
V_2 V_3 V_5
V_5
V_2
V_5
V_2
V_3
V_2
V_1 V_4
V_4
V_1
V_1 V_4
t_1
t_2
t_3
t_4
t_5

Fig. 17b

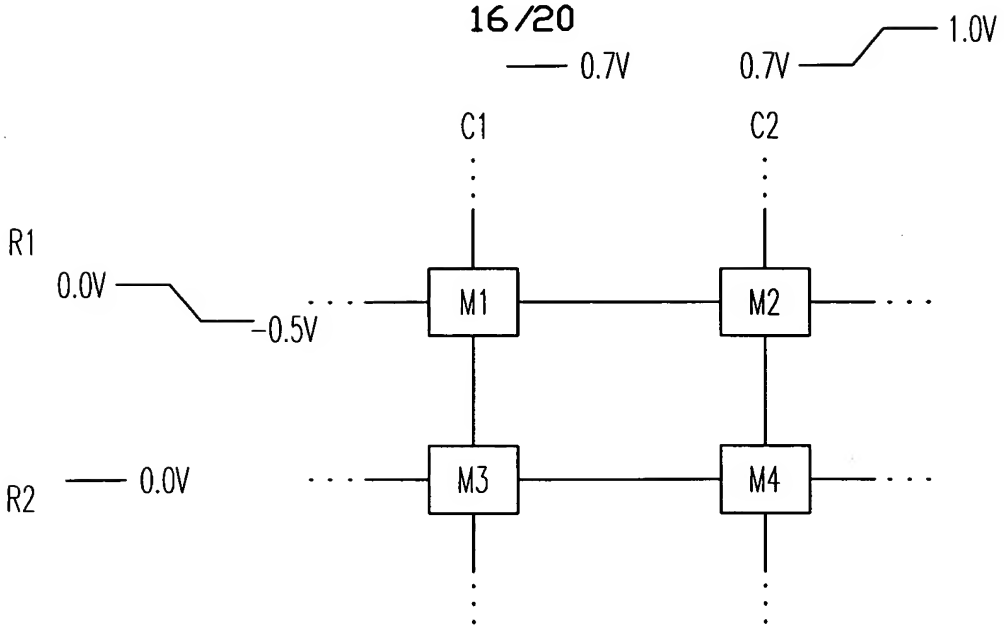

Fig. 18

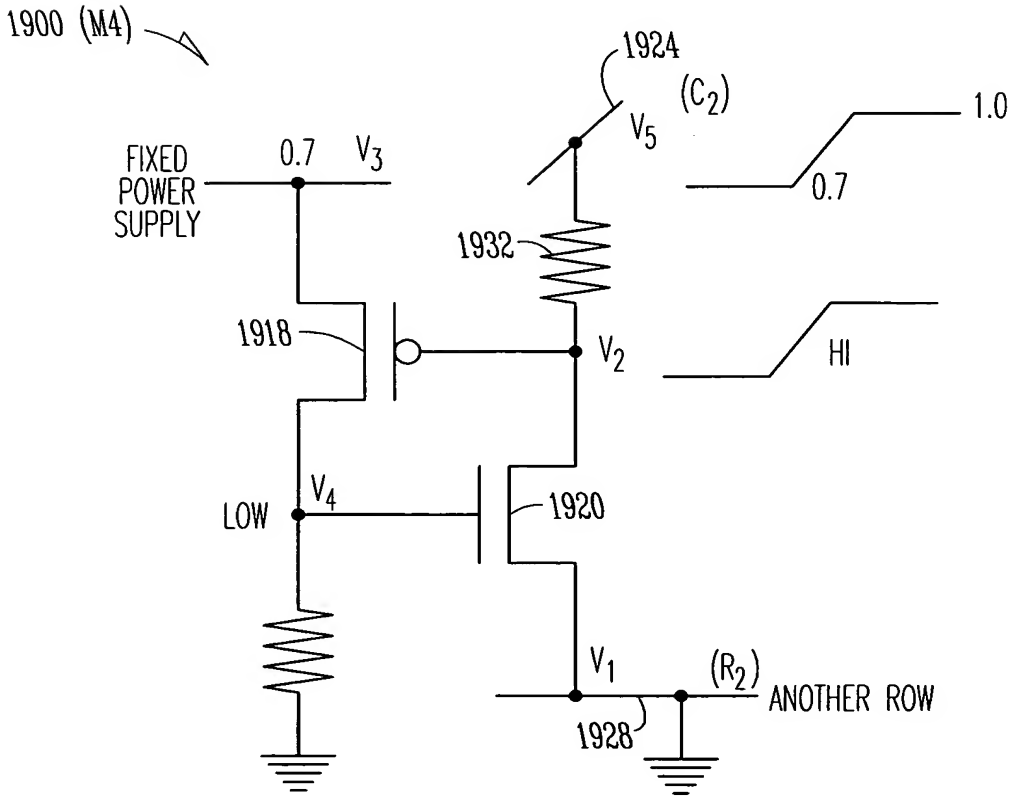

Fig. 19a

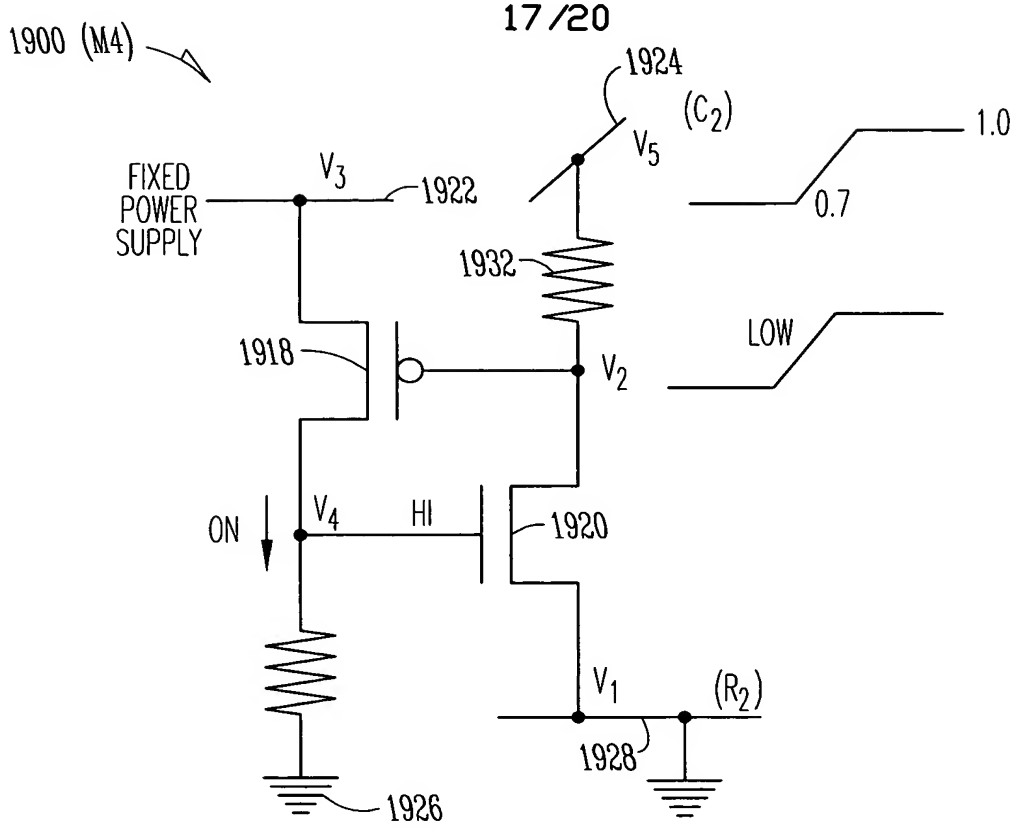

Fig. 19b

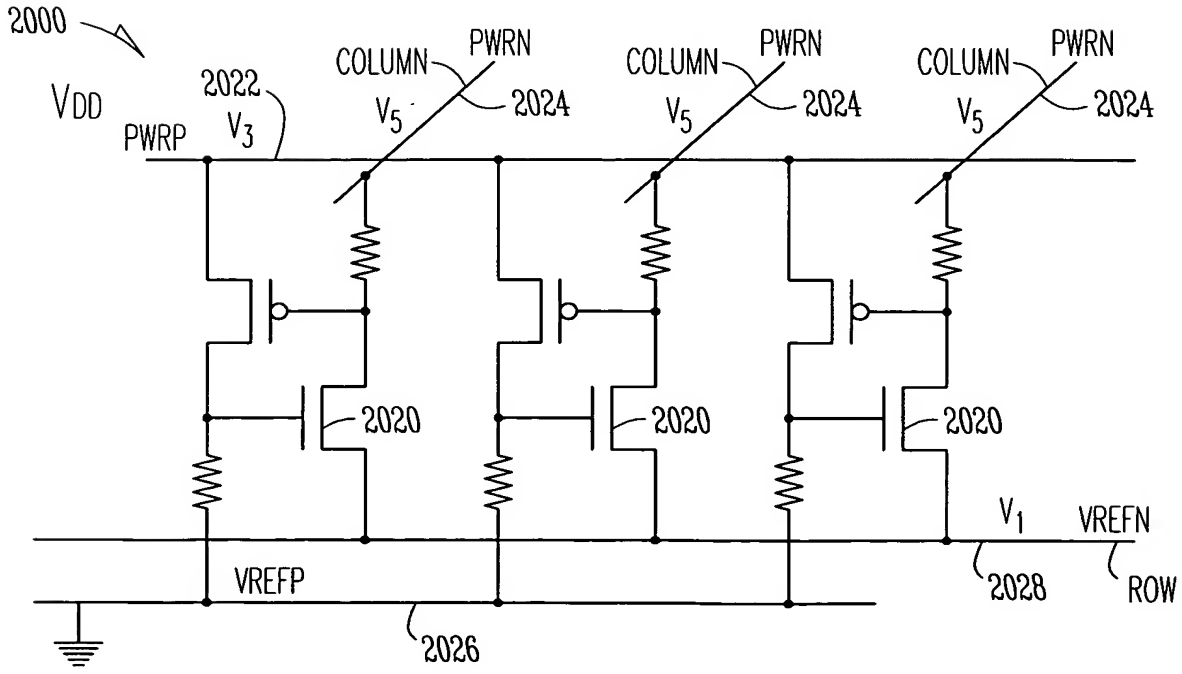

Fig. 20

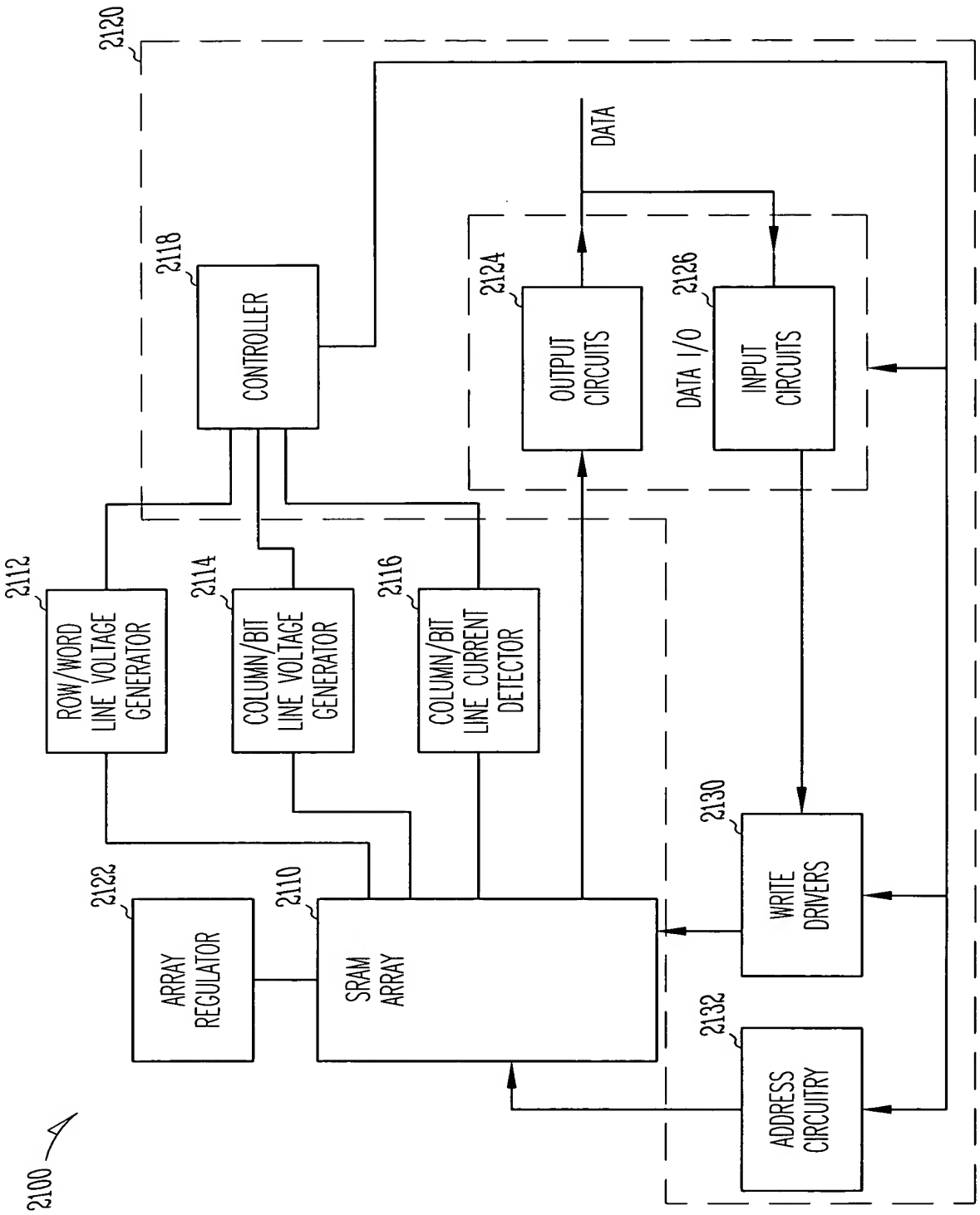
2100
2120
2118
CONTROLLER
DATA
2124
OUTPUT CIRCUITS
2126
DATA I/O
INPUT CIRCUITS
2112
ROW/WORD LINE VOLTAGE GENERATOR
2114
COLUMN/BIT LINE VOLTAGE GENERATOR
2116
COLUMN/BIT LINE CURRENT DETECTOR
2122
ARRAY REGULATOR
2110
SRAM ARRAY
2130
WRITE DRIVERS
2132
ADDRESS CIRCUITRY

Fig.21

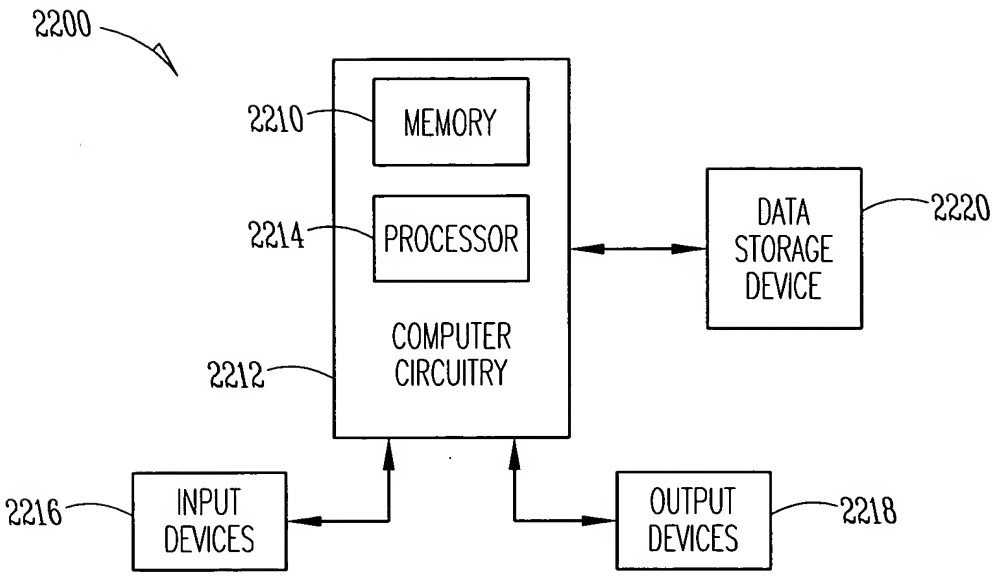
2200
2210
MEMORY
2214
PROCESSOR
COMPUTER
CIRCUITRY
2212
DATA
STORAGE
DEVICE
2220
2216
INPUT
DEVICES
OUTPUT
DEVICES
2218

Fig. 22

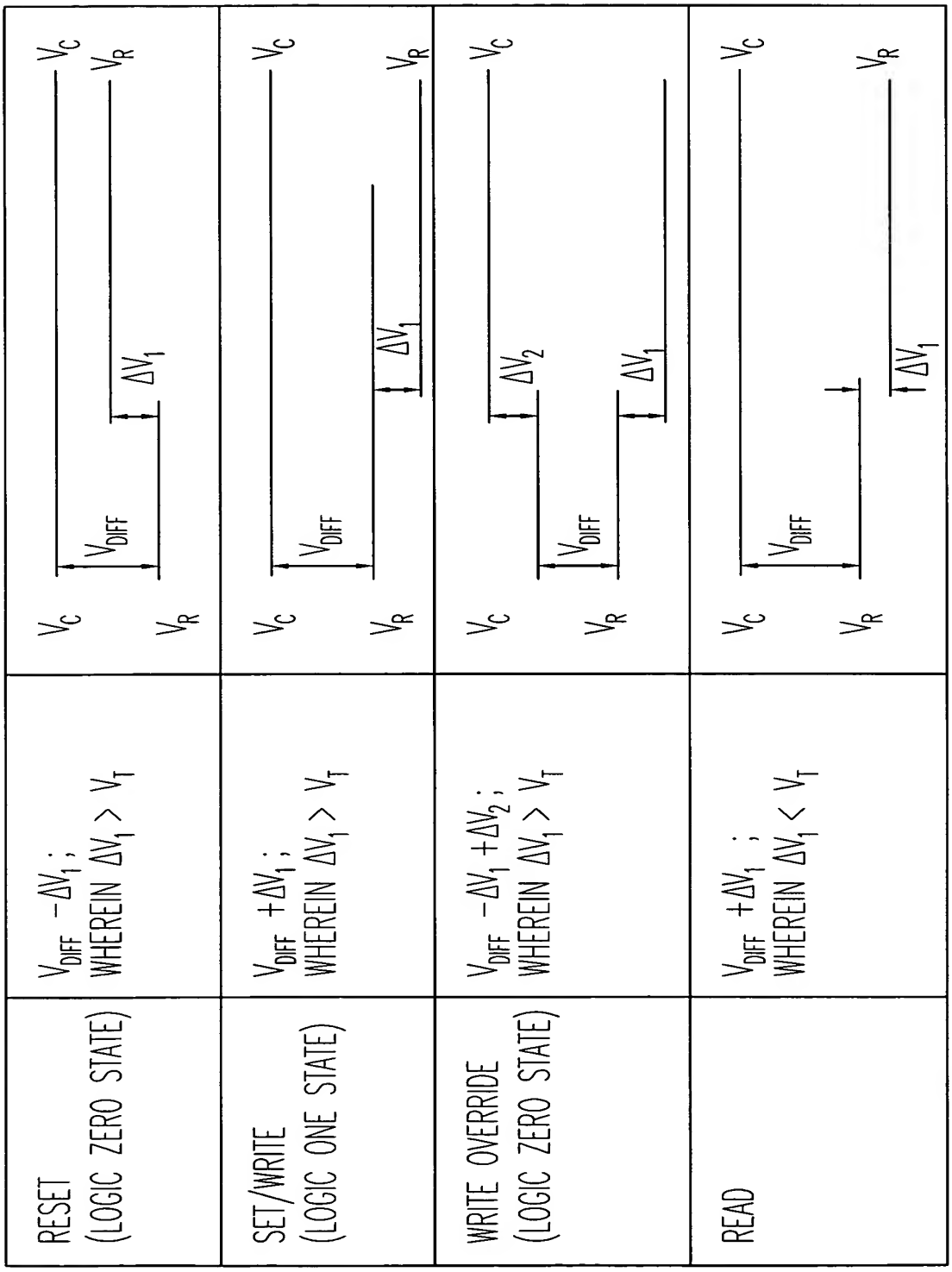
OPERATION
CONDITION
EXAMPLE
RESET (LOGIC ZERO STATE)
V_{DIFF} $-\Delta V_1$; WHEREIN $\Delta V_1 > V_T$
SET/WRITE (LOGIC ONE STATE)
V_{DIFF} $+\Delta V_1$; WHEREIN $\Delta V_1 > V_T$
WRITE OVERRIDE (LOGIC ZERO STATE)
V_{DIFF} $-\Delta V_1 + \Delta V_2$; WHEREIN $\Delta V_1 > V_T$
READ
V_{DIFF} $+\Delta V_1$; WHEREIN $\Delta V_1 < V_T$
V_C
V_R
V_{DIFF}
ΔV_1
ΔV_2

Fig.23